REMARKS

Claims 1-20 are pending in the present application and are rejected. By this response, claims 3, 17, and 19-20 are amended. No new matter has been added by these amendments. In view of the following discussion, Applicants submit that none of the claims now pending in the application are unpatentable under 35 U.S.C. §103. Thus, Applicants believe that all of these claims are now in condition for allowance.

I. OBJECTIONS

The Examiner objected to claim 20 as including an incorrect dependency. (Office Action, p. 2). Applicants have amended claim 20 to depend correctly from claim 19, as the Examiner suggested. Applicants respectfully request that the present objection be withdrawn.

II. REJECTION OF CLAIMS 1-20 UNDER 35 U.S.C. §103

The Examiner rejected claims 1-20 under 35 U.S.C. §103 as being unpatentable over U.S. Patent Application Publication 2002/0120912 filed by He et al. ("He") in view of U.S. Patent Application Publication No. 2002/0188923 filed by Ohnishi. The rejection is respectfully traversed.

More specifically, the Examiner stated that He teaches configuring configurable logic of an IC to have a plurality of thread circuits. (Final Office Action, p. 3). The Examiner cited in part paragraph 0023 of He, which states that "[i]n one embodiment, at least a first part of the IC design is interconnected on at least a first thread [and] [a]t least a second part of the IC design is interconnected on at least a second thread." After review of He in its entirety, it is clear that He's reference to "threads" is different than Applicants' "thread circuits." In particular, He describes a routing algorithm implemented in software on a computer that can be multi-threaded or single-threaded. (See He, para. 0009). That is, the software that implements the router can be multi-threaded. He is not referring to "thread circuits" implemented in configurable logic of an IC. See also He, para. 0037 ("In addition, since the routing task has been divided, multi-threaded parallelism can be applied to speed up the global router 201," and "[t]he detail router 202 can route these areas in parallel utilizing the multi-threaded parallel

computing capability of some embodiments of the present invention."), para. 0046 ("Some embodiments use the multi-threaded mechanism provided by the computer operating system to route all, or multiple, areas in parallel."), and para. 0047 ("FIG. 5 depicts an embodiment of the area-oriented, multi-threaded graph-based detail router 500."). Thus, it is clear that the "threads" in He do not teach or suggest "thread circuits," as recited in Applicants' claims.

The Examiner also cited "interconnections" in He as teaching Applicants "interconnect topology" among thread circuits. (Final Office Action, p. 3). The "interconnections" in He refer to physical routing in an IC produced by the router. See He, para. 0006, 0022. These generic interconnections in He do not teach a specific interconnection topology among a plurality of thread circuits, as recited in Applicants' claim 1.

Thus, while He uses similar language to Applicants' claims, it is apparent from the citations above that He is actually referring to traditional multi-threaded software, and not to an IC with thread circuits. Ohnishi generally teaches a logic synthesis process for circuit design. (Ohnishi, Abstract). Ohnishi does not teach or suggest configuring configurable logic of an IC to have a plurality of thread circuits and an interconnection topology among the thread circuits, as recited in Applicants' claim 1. Since neither He nor Ohnishi teach or suggest such features, no permissible combination thereof renders obvious Applicants' invention recited in claim 1.

Further, "rejections on obviousness cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." KSR Int'l Co. v. Teleflex, Inc. 82 USPQ.2d 1385, 1396 (S. Ct. 2007). There is no suggestion, motivation, or other objective reason to modify He with thread circuitry described in Ohnishi. He describes multi-threaded software for routing designs in an IC. There is no want, need, motivation, or otherwise for modifying He in order to implement specific thread circuitry in an IC. The Examiner's proposed reason for the combination of improving the efficiency of He's system is not applicable, since He does not disclose thread circuitry to which such efficiencies can be applied. Thus, a prima facie case of obviousness has not been established.

Applicants' independent claims 7, 14, and 18 each recite features similar to those emphasized above in claim 1. For the same reasons, the cited combination does not render obvious Applicants' claims 7, 14, and 18. Claims 2-6, 8-13, 15-17, and 19-20 depend from claims 1, 7, 14, and 18 and recite additional features thereof. Since the cited combination does not render obvious Applicants' invention recited in claims 1, 7, 14, and 18, the cited combination also fails to render obvious Applicants' invention recited in claims 2-6, 8-13, 15-17, and 19-20.

Accordingly, Applicants contend that claims 1-20 are patentable over the cited combination and fully satisfy the requirements of 35 U.S.C. §103. Applicants respectfully request that the present rejection be withdrawn.

CONCLUSION

Applicants submit that all of the claims presently in the application are allowable over the provisions of 35 U.S.C. §103. Consequently, Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring any action in any of the claims now pending in the application, it is requested that the Examiner telephone the undersigned at (720) 652-3733 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,

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I hereby certify that this correspondence is being filed via EFS-Web with the United States Patent & Trademark Office on August 10, 2009.

/susan wiens/
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